EmLogic

Embedded Software Hardware FPGA

Accelerating FPGA Design

*Efficiency and quality is all a question of overview, readability, extensibility, maintainability, and reuse, - and a good architecture all the way down is the answer. This applies for both Design **and** Verification*

Huge improvement potential

Digital design for FPGAs and ASICs has a huge improvement potential with respect to development time and product quality.

A lot of time is wasted on inefficient design, lack of awareness around this, and knowledge of the most critical digital design issues. This also seriously affects the quality of the end product. The good thing is that this huge improvement potential can be realised just by making a few important changes to the way we design.

This course is tool independent, technology independent and HDL independent.

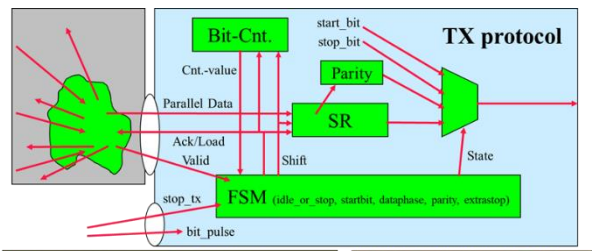
The most important design related issues to improve are:

- Design Architecture & Structure
- Clock Domain Crossing
- Coding and General Digital Design
- Reuse and Design for Reuse
- Timing Closure
- Quality Assurance - at the right level

Design Architecture and Structure

This is probably the single most important issue with respect to development efficiency and quality. Unfortunately most FPGA modules are not at all properly structured. There is of course always some kind of structure, but often not even close to a good and efficient structure. This course looks at the details of some "standard" bad and a desired good design structuring. Architecture is key at all levels from top level to deep down into the module micro architecture.

A good design structure yields a good overview and understanding, easier extendibility and maintainability, and far better modification and reuse capability. A very important side effect is lower power consumption, better frequency performance and a smaller FPGA/ASIC footprint.

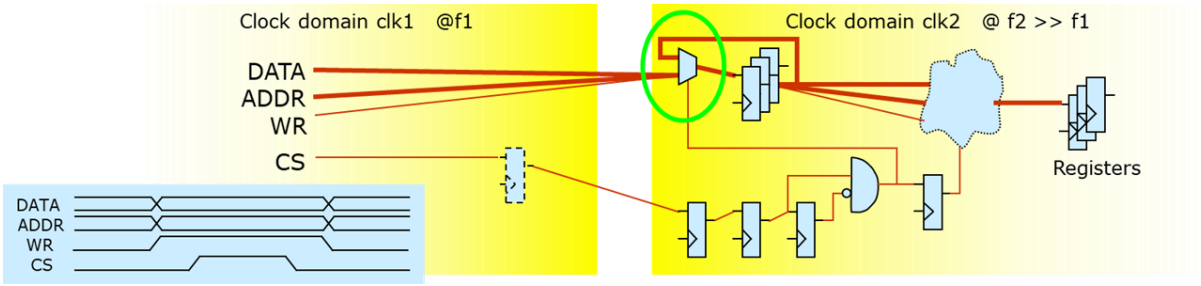


- Clean interface towards data sources (Data + Valid + ACK)
- Number of sources or priorities not of interest
- Controlled handshakes and "feed forward"
- Far less input signals to FSM.
- Passive Data-path. No data/FSM interaction.

- Much simpler to understand.
- Simpler debug and less risk.
- Probably less area and power.
- Less verification. Simpler STA.
- Repeat for all stages...

Clock Domain Crossing (CDC)

CDC is one of the most error prone areas of digital design. Most designers believe they know how to handle this perfectly well, - but for some strange reason this is still the worst problem in a lot of projects. What we often see is that a CDC was not as trivial as first assumed. There are lots of special cases where you need to know exactly how to handle a specific challenge for a specific technology/device given your specific synthesis and P&R tool. This course looks at general CDC issues and how to handle them, but also looks closer at a lot of special scenarios.



Coding and General Digital Design

Coding style is very individual, and to a certain extent that is acceptable. However, most coding styles are not really acceptable or good enough if you are considering readability, understanding and maintenance, and thus not at all acceptable with respect to efficiency and quality. This course looks at how to write understandable and modifiable code.

There are some myths and misunderstandings around FSM coding and Reset handling. We will have a closer look at that in this course.

Registers are defined and described multiple places like C header files, HDL design files, HDL Testbench and Documentation. This should really be generated and maintained automatically to save time and keep all parts synchronized. We will show one way of handling this.

This section will show examples in VHDL, but 80-90% applies equally well to Verilog.

Reuse and Design for Reuse

Actually Reuse and Design for Reuse are two totally different subjects.
The course will look at the following:

- Design for 'Plug and Play' reuse
- Wrapping for 'Untouched reuse'
- Design for modified reuse

All of these aspects have different challenges and benefits, and we will go into some details on that.

Timing Closure

The course will not dive into technology specific optimization, but will look at how performance may be improved by applying a more structured architecture.

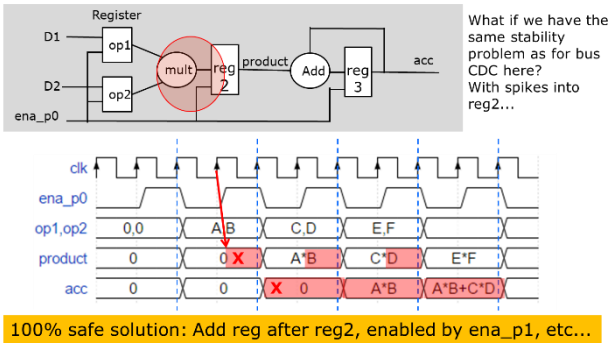
Verification

This course will not look at Verification architecture, structure or language, which is all properly covered in a separate course 'Advanced VHDL Verification – Made simple', but will briefly look at some selected verification issues.

Quality Assurance - at the right level

Most quality issues will be covered while discussing architecture, CDC, and coding, but the course will also look at how quality may be improved by walk-through, sparring, reviews, checklists, checklist handling, conventions, documentation etc.
(For Conventions VHDL will be used as example)

Potential Multicycle problem



Target audience and prerequisites

The course is intended for FPGA designers and Digital ASIC designers who wants to work smarter and more efficiently - and design products with higher quality. Participants should have a good knowledge of FPGA development. Less experienced designers will also benefit significantly from this course, but will have less relation to the critical aspect of FPGA Development Best Practices.
Previous participants have had from 1 year to 30 years' experience.

Main Benefits

The main goal of this course is to show how you can develop a far better FPGA/ASIC design – especially with respect to design overview, architecture, readability, extensibility, maintainability and reuse – resulting in better quality and faster development. Additionally typical pitfalls will be covered – with a special focus on timing, synchronization, resets and clock domain crossing.

In General

There will be a few examples on quite common bad design approaches- as this is very useful as an eye opener, - and then of course more examples on good approaches for architecture, CDC, Coding, Reuse, etc.

The main focus in this course is quality and efficiency improvement, making you a better designer and your company a better product development organisation.

80-90% of the course is HDL independent. VHDL is used where code examples are needed, but most of this will be directly transferable to Verilog or SystemVerilog.

The presentation and material will be in English.

Presenter

Presenter and lab instructor at this course is Espen Tallaksen, the main architect behind UVVM.

Espen is the CEO and founder of the newly established EmLogic and previously also Bitvis, both independent design centres for embedded software and FPGA, - with Bitvis as a leading Nordic company within its field and EmLogic soon to be. He graduated from the University of Glasgow (Scotland) in 1987 and has 30 years' experience with FPGA and ASIC development from Philips Semiconductors in Switzerland and various companies in Norway. For twenty years Espen has had a special interest for methodology cultivation and pragmatic efficiency and quality improvement. One result of this interest is the UVVM verification platform that is the #1 VHDL verification methodology and library world-wide, and in fact the fastest growing FPGA verification methodology independent of HDL.

He has given many presentations and keynotes internationally on various technical aspects of FPGA development, including lots of hands-on tutorials and presentations at FPGA-Kongress every year since 2016; - all with a crowded audience and great feedback. He is also giving courses world-wide on how to design and verify FPGAs more efficiently and with a better quality.
The fundamental message is always the same: Overview, Readability, Extensibility, Maintainability and Reuse are the key elements to Quality and Efficiency. Overly complicated design or verification systems should be avoided – even when they are structured. Simplicity – to the extent possible - should always be the target for any challenge.

Quotes from previous courses:

- The only bad thing about this course - is that we didn't do it earlier
- An eye opener - Most issues apply directly in our organisation
- A very good course on very relevant improvement potentials
- I think the material is need-to-know for every designer
- The course makes you think through how you and your company are doing things

Other info:

This course is complementary to the courses offered by FPGA vendors and tool vendors - and also complementary to more general courses offered by Doulos and various universities. The strong focus on the issues that matter the most for efficiency and quality makes this a good platform for a pragmatic approach to improving your FPGA and ASIC projects.

This course may also be held on-site on request - with a duration of one to three days depending on your starting point and level of ambition. Such a course allows some flexibility and adaptation - and would promote more interaction.

Registration:

If you received an invitation to this course from one of our course partners, please register via them (unless you have been told otherwise).

Otherwise please register to info@emlogic.no and give the following information: Name, Company name, Company Address, Email, Mobile, – and if required by your company - a Purchase order reference.